New Techniques for Analysis, Validation, and Debug of High Speed DDR Memory

Presented by:
Jennie Grosslight
Memory Product Manager
Agilent Technologies
Agenda

• Overview of DDR Debug and Validation
• Real-Time protocol Violation Detection Techniques
• Bus Level Signal Integrity Insight using DDR EyeScans
• Summary
• Q&A
Overview of DDR/2/3/4 LPDDR/2/3/4

Debug and Validation

Power On Test
- Scope Signal Integrity
- Basic Compliance (i.e., clock, voltages)
- Logic analyzer
  State and Timing mode traces
- Bus Level Signal Integrity Insight

Legend
- Logic Analyzer
- Scope

Boots may be unstable

Logic Analyzer
State and Timing mode traces

System Functionality
- SW Integration (drivers)
- Cross-bus traffic
- Performance tuning
- Real Time Protocol Violation Detection
- Bus Level Signal Integrity Insight

OS boots up

Boot Sequence
- Memory training/initialization
- Cycle level timing characterization
- Bus Level Signal Integrity Insight
- Real Time Protocol Violation Detection
- Failure Analysis - Subsystem / signal Isolation

Live application / stress

Root cause parametric failure analysis
- Detailed parametric characterization
- Compliance / Vendor qualification
Validating and Debugging DDR Memory: Logic Analyzer test and validation techniques

Timing Modes:
- Timing Mode
- Transitional Timing
- 12.5GHZ Timing Zoom

State Mode Functional Validation:
- Setup Assistant
- MRS
- Decode
- Burst Triggering
- Post process Compliance tools

Real time Violation Testing
- Monitor DDR/2/3/4 and LPDDR2/3
- Customizable tool for other buses

Bus Level Signal Integrity Insight
- Qualitative comparison of qualified eye scans using the Agilent logic analyzer
Basic Requirements for Logic Analyzer
DDR2/3/4 and LPDDR2/3/4 Solutions

Connect  Acquire  View & Analyze

Interposers

BGA Probes

Mid-Bus Probing

U4154A
4 Gb/s  2.5Gb/s Ultra High Speed Logic Analysis Module
2.5GHz Trigger Sequencer

DDR Decoders
DDR Protocol Compliance
Performance Analysis
Trigger Tool

Bus Level Signal Integrity Insight
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• Overview of DDR Debug and Validation

• Real-Time protocol violation detection techniques
  • Post Process vs. Real-Time
  • Real-Time Compliance SW tools on the logic analyzer
    • Real-Time external probe – DDR Detective

• Bus Level Signal Integrity Insight using DDR eye scans

• Summary

• Q&A
Post Process vs. Real-Time Violation Detection

**Biggest difference:** Post process is limited to trace depth.

- Typically milliseconds to maximum of a few seconds

**Real-Time:** user selects coverage time

- seconds, minutes, hours ……

New repetitive run on Post Process tool provides “concurrent real-time” violation detection. Improves statistical accuracy of post process results. It isn’t “Real-Time”.

Typical coverage using post process methods:

- 100ms
- 1 sec
- 30 sec
- 5 min
Post Process Benefits

... Why use if Real-Time is available?

- Quick check of Logic Analyzer trace for possible violations
- Easy method to check a trace of a system crash
- Typically optional SW tool on logic analyzer

Example:
Time out trigger to capture trace of system crash

DDR system stops writing to memory when system crashes
New repetitive run on Post Process tool provides “concurrent real-time” violation detection.

- Post Process results example
- Run on logic analyzer trace
Post Process vs. Real-Time Violation Detection .....continued

Real-Time Benefits

• Monitor DDR traffic for protocol violations
  • User defines length of time for testing
    • Parts per million accuracy increases with monitoring time

• Automatically triggers on violations

• Automatically captures trace of each violation
Real-Time Compliance SW tool on Logic Analyzer

- Select technology
- Customizable tests

### Automated Validation Tool

#### Setup

- **Run Options**
- **Run/Results**

#### Manage Test Groups

<table>
<thead>
<tr>
<th>Test Group Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3 Tests</td>
<td>Compliance tests for DDR3</td>
</tr>
<tr>
<td>DDR4 Tests</td>
<td>Compliance tests for DDR4</td>
</tr>
<tr>
<td>LPDDR2 Tests</td>
<td>Compliance tests for LPDDR2</td>
</tr>
<tr>
<td>LPDDR3 Tests</td>
<td>Compliance tests for LPDDR3</td>
</tr>
</tbody>
</table>

#### Select Tests to Run

- **Test Selection Shortcuts**

#### Test Time

- Enter the amount of time to run each test: Hours: 0, Minutes: 5, Seconds: 0
- Total Estimated Test Run Time: 5 Hours 20 Minutes

#### Customize Tests

<table>
<thead>
<tr>
<th>Target Speed</th>
<th>tRCD (ns)</th>
<th>tRP (ns)</th>
<th>Clocks</th>
<th>LA asserts</th>
</tr>
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<tbody>
<tr>
<td>800MHz</td>
<td>5</td>
<td>13.5</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>1066MHz</td>
<td>6</td>
<td>11.25</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>1333MHz</td>
<td>7</td>
<td>9.64</td>
<td>7</td>
<td>14</td>
</tr>
<tr>
<td>1600MHz</td>
<td>8</td>
<td>8.84</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>1866MHz</td>
<td>9</td>
<td>8.39</td>
<td>9</td>
<td>18</td>
</tr>
<tr>
<td>2133MHz</td>
<td>11</td>
<td>7.97</td>
<td>11</td>
<td>20</td>
</tr>
</tbody>
</table>

**Note:**
- For all defined combinations of target speed and CAS latency, tRCD and tRP are simply equal to the CAS latency.
- To override this setting, either apply the appropriate test group parameter values file, or manually override the value below.

- **Default value:** 28
- **Manually override value of tRCD and tRP**
- **Enter value for tRP and tRCD (in LA states):** 28

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**Anticipate — Accelerate — Achieve**

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Real-Time Compliance SW tools on Logic Analyzer

- Select Run options
- Run
- View Violation results

- Traces of violations saved in directory of your choice.
- Open Violation traces to view details
Real-Time Compliance SW tools on Logic Analyzer

Real-Time trace example:
Trigger on tRCD violation
Write too close to Activate
Customizable tests with logic analyzer Real-Time Compliance Toolset.

Editeable parameters on existing test groups for JEDEC specified data rates

- Default State mode configurations for
  - DDR4
  - DDR3
  - DDR2
  - DDR
  - LPDDR3
  - LPDDR2
  - LPDDR

Create your own unique test groups for custom regression tests.

- Create a different test group for each Agilent logic analyzer configuration.
  - Any system that can be probed by your Agilent logic analyzer.
  - Any valid Agilent logic analyzer trigger.
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  • Real-Time Compliance SW tools on the logic analyzer
  • Real-Time external probe – DDR3 Detective
• Bus Level Signal Integrity Insight using DDR eye scans
• Summary
• Q&A
Real Time Protocol Violation detection:

– Monitor hundreds of protocol parameters simultaneously
– Capture full traces of ADD/CMD/DATA on logic analyzer
– Scope Trigger specific signals of interest

FuturePlus DDR3 Detective with Agilent U4154A Logic Analyzer
Real Time Violation Detection Example: Bus Contention

- Write followed too quickly by a Read to the same RANK #S1
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- Bus Level Signal Integrity Insight using DDR eye scans
  - Signal integrity insight for setting State mode sample positions
  - DDR eye scan overlay mode signal integrity insight examples
  - DDR eye scan burst scan mode signal integrity insight examples
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Bus Level Signal Integrity Insight:

- Bridging a measurement gap

**Design**
EEsof EDA

**Signal Integrity**
Infinium 90000 Series Scope
InfiniiMax Probes

**Functional Analysis and Validation**

Plus Bus Level Signal Integrity Insight

U4154A Logic Analyzer Module
In M9502A Chassis

5ps x 2mV Sample position resolution

Bus Level Signal Integrity Insight
Two Bus Level Signal Integrity Views

Overlay Mode

- Required to set State mode sampling positions
- Rapid Bus level signal integrity insight

Burst Scan Mode (Signal Trace Mode)

- Unique qualified scan views
- Simultaneous views of all DQS
- Bubble Scans
Overlays clock delayed copies of 4 or 8 bursts on top of each other.

Results in one good eye opening

Used to:

• Set best sampling position for State mode measurements
• Bus Level Signal Integrity Insight
Setting the most accurate sample position is becoming more critical:

**Data Valid Windows Shrinking**
- Data Rates Increasing
- Voltage levels decreasing

Data valid windows scanned on logic analyzer from DDR3 and DDR4 DIMM interposers.
DDDR4 eye scan example

- Scan trigger setup in default configuration
- Runs automatically from DDR Setup Assistant tool

DDR4 Bank group 1 Transitioning incorrectly
Example: Bus Level Signal Integrity Insight

DDR3 1867 DIMM

Eyes for Byte lane 1 are larger than Byte lane 2
Example: Bus Level Signal Integrity Insight

DDR3 1867 DIMM
Eyes for DQS1 are cleaner than DQS2
Overlay mode: Example #1 summary

DDR3 1867 DIMM
DQS 2 eye is smaller than DQS1

DDR3 2340 DIMM Eyes all DQS eyes are larger/cleaner than DDR3 1867 DIMM eyes
Comparing 1.6V vs. 1.2V operation of the same signals on the same system at the same data rate helps identify areas of weakness for achieving higher signal swings at lower voltages.

Fall time on CAS at 1.2V appears to be sluggish compared to the scan at 1.6V.
Read Data: 1.6 V vs. 1.2 V Operation

1.6V Read eyes
Threshold = User
vThresh = 778.7 mV
tSample = 810 ps

Threshold = User
vThresh = 784 mV
tSample = 859 ps

Threshold = User
vThresh = 804 mV

1.2V Read eyes
Threshold = User
vThresh = 610 mV
tSample = 810 ps

Threshold = User
vThresh = 584 mV
tSample = 859 ps

Threshold = User
vThresh = 582 mV
Two Bus Level Signal Integrity Views

Overlay Mode

• Required to set State mode sampling positions
• Rapid Bus level signal integrity insight

Burst Scan Mode (Signal Trace Mode)

• Unique qualified scan views
• Simultaneous views of all DQS
• Bubble Scans
Bus Level Signal Integrity Insight:

– Burst Scan mode (Signal Trace Mode)

Overlaying identically clocked copies of 4 or 8 bursts on top of each other (Burst Scan mode)

Used for specialty scans: Scans built in sequence.
Open up DQS eyes with Burst Scan (Signal Trace mode)

- Observe preamble
- Compare relative DQS quality
- Compare traces taken under different conditions
- or with different components.

DDR3 2340 DIMM DQS eyes scanned with Burst Scan (Signal Trace mode)
Burst Scan - Bubble Scan Example

Logic Analyzer can provide unique triggered scans on bubble between bursts

Note inconsistent tri-state behavior on last sample in 1st burst.

• Next step, a trigger can be prepared on the LA to capture bubble bursts of one cycle between the suspect ranks and cross trigger the scope.
Example: Investigating ISI

DDR eyescan customized view – Signal Trace Scan

- Intersymbol interference plainly visible
- Protocol triggering can isolate
Use View Scope to investigate further

Setup LA Trigger for bit pattern that stresses ISI:

- Data bit pattern 00101
- Capture DQS and DQ with scope
- View scope traces in LA display to correlate functional with Signal Integrity trace from scope.
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Summary – New logic analyzer tools

Save time and increase insight for DDR/2/3/4 and LPDDR/2/3 debug and validation:

- **Real-Time protocol violation testing**

- **Bus level signal integrity insight**
More slides with additional information on Agilent DDR/2/3/4 and LPDDR/2/3/4 Memory Test Solutions
For video Demo series:
www.agilent.com/find/logic-analyzer-videos

To learn more about the U4154A logic analyzer go to:
www.agilent.com/find/U4154A
U4154A Typical DDR4 DIMM Configuration

- Two U4154A logic analyzer modules
- M9502A 2 slot AXIe chassis
- User-supplied Host PC
- PCI Express Cable and adapter
- FS2501B DDR4 DIMM interposer with seamless cable connections to U4154A
- DDR4 System under test
- Logic Analyzer System SW common to:
  - U4154A
  - 16900 series
  - 16800 series
  - PCI Express Gen3 HDMI
**DDR4 Interposers**

- Ease of connection
  - Direct connect to U4154A
- Low profile - Minimal loading
- Supports UDIMM or RDIMM
- Timing and State analysis
- Includes FuturePlus protocol decoder to show executed bus transactions
- Supports DDR Setup Assistant and DDR EyeScans

**FS2501B:** DDR4 2400 DIMM interposer

**FS2502B:** DDR4 1867 SODIMM interposer

*Agilent Technologies*
U4154A Typical Configuration for DDR3 DIMM

System SW common to:
- U4154A 16900 series
- 16800 series
- PCI Express Gen3
- HDMI

User-supplied PC

System under test

M9502A AXIe chassis

Probing to system under test

PCI Express Cable and adapter

U4154A

U4201A cables
DDR SW tools

✓ **B4622B** enhanced compliance toolset:
  ✓ Enhanced LPDDR/2/3 violation measurements
  ✓ Enhanced DDR2/3/4 violation measurements
  ✓ New ‘ Concurrent Real Time’ violation detection with repetative run feature on post process violation tool.
  ✓ New ‘Real Time – One at a Time’, Automated Validation Tool
  ✓ New custom violation measurement capability
    ✓ quick turn solutions for new memory technologies and general purpose targets!

✓ **B4623B** LPDDR/2/3 decoder = new coverage for LPDDR3!

✓ **B4621B** DDR2/3/4 decoder = new coverage for DDR4!
## DDR Memory Probing Solutions

<table>
<thead>
<tr>
<th></th>
<th>DDR2</th>
<th>DDR3</th>
<th>LPDDR / LPDDR2/LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>200 Mb/s ~ 800 Mb/s</td>
<td>800 Mb/s ~ 2133 Mb/s</td>
<td>200 Mb/s ~ 1600 Mb/s</td>
</tr>
<tr>
<td>DIMM Interposer</td>
<td>FuturePlus FS2334 (~800)</td>
<td>FuturePlus FS2352 (~2133)</td>
<td>NA</td>
</tr>
<tr>
<td>SO-DIMM Interposer</td>
<td>FuturePlus FS2337 (~667)</td>
<td>FuturePlus FS2354 (~1600)</td>
<td>NA</td>
</tr>
<tr>
<td>BGA probes</td>
<td>W2631B (x16), W2633B (x8) E5384A (ZIF cable)</td>
<td>W3631A (x16) W3633A (x8) E5845A (ZIF cable for x16) E5847A (ZIF cable for x8)</td>
<td>W2637A (x16), W2638A (x32) (LPDDR), Custom (LPDDR2)</td>
</tr>
<tr>
<td>Mid-bus</td>
<td>E5406A SoftTouch Pro</td>
<td>E5406A SoftTouch Pro</td>
<td>E5406A SoftTouch Pro</td>
</tr>
<tr>
<td>Others</td>
<td>W2639A DDR2/DDR3/ LPDDR Scope Adaptor Board</td>
<td>W2635A (x8), W2636A (x16) DDR3 Scope only BGA Probe W3635A DDR3 Scope Adaptor Board</td>
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## Shared Scope & Logic Analyzer Probing

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<th>BGA probes and scope adapter boards</th>
<th>DDR2</th>
<th>DDR3</th>
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### Tip resistors
Tip resistors connect to E5381A Differential flying leads or 1134A InfiniMax

### Mid-bus
E5406A SoftTouch Pro

N2887A Soft Touch Pro to InfiniiMax probe head adapter for use with scope.