MIPI D-PHY Protocol Fundamentals
Scope of this discussion

Mobile Computing
D-PHY Protocols
• D-PHY Layers
• Signaling and Traffic
• HS and LP Modes
• D-PHY States
• CSI and DSI idiosyncrasies

Early view of MIPI M-PHY
Demonstration of D-PHY Protocol Tools
Demand is shifting from client/laptop devices to smart devices.

Meanwhile, laptop devices will start to look more like smart devices.

– PC demand is flattening and moving to mobile computing

“The cloud computing market is heading into the stratosphere as companies seek to offer services designed to serve tablets, smartphones and other mobile devices. … projected to surge to $110 billion in 2015, up from $23 billion in 2010.”

iSuppli December 22, 2011
## MIPI Layered Protocols

### Application
- Camera Interface
- Display Interface
- Radio Interface
- Storage Interface

### Protocol Standard
- CSI-2
- DSI/DCS
- DigRF v4
- CSI-3
- UFS
- UniPro
- LLI
- SSIC
- M-PCIe

### Physical Standard
- D-PHY
- M-PHY
MIPI Monolithic Protocols & Applications
About the MIPI Alliance

Coordinate technology across the mobile computing industry

- Over 240 member companies
- 100% penetration of MIPI specs in smartphones by 2013

Develop specifications that ensure a stable, yet flexible technology ecosystem

- 17 official working groups (14 active) and growing
- Partnerships with other industry organizations (JEDEC, USB-IF, Open Mobile Alliance, 3GPP, MEMS, etc.)
- Only members have access to specifications
- All members can participate and vote in discussions; higher levels of membership required to lead.
D-PHY layers (DSI example)
D-PHY Signaling Highlights

1-4 Data Lanes (trying to push the spec to x8)
  - 1 lane clock for all data lanes
2 types of signaling LP and HS
  - LP P & N signals are driven independently
  - HS is differentially driven

Primarily a unidirectional link

Can get reverse communication though a Bus Turn Around (BTA) for DSI
D-PHY
Global Operation Flow Diagram

TX
- Init Master
- LS-PD: LP-00
- LS-PD: LP-01
- Stop LP-11
- LP-Rqst LP-10
- EoT
- HST
- SoT

RX
- Init Slave
- LS-PD: LP-00
- LS-PD: LP-01
- Stop LP-11
- LP-Rqst LP-10
- EoT
- HST
- SoT
- Escape Mode

Turnaround LP-00>10>00>10

Agilent Technologies
D-PHY Low Power Signaling

LP Control
- 1.2V Nominal
- Stop state LP-11
- Escape Mode & HS Mode Entry/Exit
- Bus Turnaround (BTA), [DSI]

Escape Entry Codes
- Trigger/Modes (generic protocol messaging)
- Ultra Low Power (ULP – 78h)
- Low Power Data Transmission (LPDT – 87h)
- Derived clock, 10Mbs max.

Binary opposites
High-speed to Low-power transitions in action

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>Time</th>
<th>MIPI-DSI Packet</th>
<th>Data ID</th>
<th>Short Packet Data 0</th>
<th>Short Packet Data 1</th>
<th>ECC</th>
<th>Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>396</td>
<td>10.343250 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>397</td>
<td>10.347056 ms</td>
<td>PPS 24b RGB 8:8:8 (HS)</td>
<td>3E</td>
<td>00</td>
<td>00</td>
<td>15 (GOOD)</td>
<td>3E</td>
</tr>
<tr>
<td>398</td>
<td>10.348186 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>399</td>
<td>10.400203 ms</td>
<td>PPS 24b RGB 8:8:8 (HS)</td>
<td>3E</td>
<td>00</td>
<td>00</td>
<td>15 (GOOD)</td>
<td>3E</td>
</tr>
<tr>
<td>400</td>
<td>10.446154 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>401</td>
<td>10.451658 ms</td>
<td>PPS 24b RGB 8:8:8 (HS)</td>
<td>3E</td>
<td>00</td>
<td>00</td>
<td>15 (GOOD)</td>
<td>3E</td>
</tr>
<tr>
<td>402</td>
<td>10.497610 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>403</td>
<td>10.503126 ms</td>
<td>PPS 24b RGB 8:8:8 (HS)</td>
<td>3E</td>
<td>00</td>
<td>00</td>
<td>15 (GOOD)</td>
<td>3E</td>
</tr>
<tr>
<td>404</td>
<td>10.549066 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>405</td>
<td>10.600552 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>406</td>
<td>10.603226 ms</td>
<td>H Sync Start (HS)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
<tr>
<td>407</td>
<td>10.704708 ms</td>
<td>H Sync Start (LP)</td>
<td>21</td>
<td>00</td>
<td>00</td>
<td>12 (GOOD)</td>
<td>21</td>
</tr>
</tbody>
</table>

**Waveform**

- **DSI-102-MIPI-DSI Packet**
- **DSI-102-R.DO_LP_p**
- **DSI-102-R.DO_LP_n**
- **DSI-102-R.DO_HS**

**Sync Event V Sync Start (LP)**

- **ESC**: 11 10 00 01 00
- **LPDT**: 87h
- **Data ID**: 01h
- **Data 0**: 00h
- **Data 1**: 00h
- **ECC**: 07h

**Mark-1 & Stop**: 00 09 10 11

*Image courtesy of Agilent Technologies.*
Bus Turnaround Procedure

- Only used on DSI
- Restricted to LP mode
- One lane only
BTA in action

Processor to Peripheral

Peripheral to Processor is identical
D-PHY High Speed Signaling

- Source-synchronous clocking, dual data rate
- Differential 200mV Nominal, Common Mode 200mV, nominal
- 80Mbs to 1.5Gbs (clock rates from 40MHz to 750MHz)
- Used for payload transmission
HS Burst in action
ECC error correction (both short and long packets)

Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

- Includes both the Data Identifier and Word Count fields
- Hamming Code
  - Detects 2-bit errors
  - Recovers 1-bit errors
Checksum (long packets only)

Payload portion of long packets

Functionality:
- 16-bit field (covers 64k payload)
- Can only indicate the presence of one or more errors in the payload.
- Cannot be used to correct errors.

Usage:
- Mandatory for processor to peripheral communication (DSI).
- Optional for peripheral to processor. If not used, “0000h” checksum must be sent.
- If the payload length is 0, checksum is “FFFFh”
Packet Formats

Short Packets:
- 4-byte packets

Data Identifier lists different types of packets:
- Sync Events
- EoT
- Commands
- Generic Short Writes
- Generic Short Reads
- Short DCS command data (DSI)
- ACKs and Error Reports

Can be HS or LP
Many codes are reserved for future use
Packet Formats

Long Packets:
- 4-byte header
- Up to 64k byte payload
- Word Count identifies length.

Data Identifier lists different types of packets:
- Blanking
- Generic Long Writes
- Image Data
- DCS command data (DSI)
- Response from Peripheral (DSI)

Can be HS or LP
Many codes are reserved for future use
Example: DSI Packets

<table>
<thead>
<tr>
<th>Data Type, hex</th>
<th>Data Type, binary</th>
<th>Description</th>
<th>Packet Size</th>
<th>Data Type, hex</th>
<th>Data Type, binary</th>
<th>Description</th>
<th>Packet Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h</td>
<td>00 0001</td>
<td>Sync Event, V Sync Start</td>
<td>Short</td>
<td>24h</td>
<td>10 0100</td>
<td>Generic READ, 2 parameters</td>
<td>Short</td>
</tr>
<tr>
<td>11h</td>
<td>01 0001</td>
<td>Sync Event, V Sync End</td>
<td>Short</td>
<td>05h</td>
<td>00 0101</td>
<td>DCS WRITE, no parameters</td>
<td>Short</td>
</tr>
<tr>
<td>21h</td>
<td>10 0001</td>
<td>Sync Event, H Sync Start</td>
<td>Short</td>
<td>15h</td>
<td>01 0101</td>
<td>DCS WRITE, 1 parameter</td>
<td>Short</td>
</tr>
<tr>
<td>31h</td>
<td>11 0001</td>
<td>Sync Event, H Sync End</td>
<td>Short</td>
<td>06h</td>
<td>00 0110</td>
<td>DCS READ, no parameters</td>
<td>Short</td>
</tr>
<tr>
<td>08h</td>
<td>00 1000</td>
<td>End of Transmission (EoT) packet</td>
<td>Short</td>
<td>37h</td>
<td>11 0111</td>
<td>Set Maximum Return Packet Size</td>
<td>Short</td>
</tr>
<tr>
<td>02h</td>
<td>00 0010</td>
<td>Color Mode (CM) Off Command</td>
<td>Short</td>
<td>09h</td>
<td>00 1001</td>
<td>Null Packet, no data</td>
<td>Long</td>
</tr>
<tr>
<td>12h</td>
<td>01 0010</td>
<td>Color Mode (CM) On Command</td>
<td>Short</td>
<td>19h</td>
<td>01 1001</td>
<td>Blanking Packet, no data</td>
<td>Long</td>
</tr>
<tr>
<td>22h</td>
<td>10 0010</td>
<td>Shut Down Peripheral Command</td>
<td>Short</td>
<td>29h</td>
<td>10 1001</td>
<td>Generic Long Write</td>
<td>Long</td>
</tr>
<tr>
<td>32h</td>
<td>11 0010</td>
<td>Turn On Peripheral Command</td>
<td>Short</td>
<td>39h</td>
<td>11 1001</td>
<td>DCS Long Write/write_LUT Command Packet</td>
<td>Long</td>
</tr>
<tr>
<td>03h</td>
<td>00 0011</td>
<td>Generic Short WRITE, no parameters</td>
<td>Short</td>
<td>0Eh</td>
<td>00 1110</td>
<td>Packed Pixel Stream, 16-bit RGB, 5-6-5 Format</td>
<td>Long</td>
</tr>
<tr>
<td>13h</td>
<td>01 0011</td>
<td>Generic Short WRITE, 1 parameter</td>
<td>Short</td>
<td>1Eh</td>
<td>01 1110</td>
<td>Packed Pixel Stream, 18-bit RGB, 6-6-6 Format</td>
<td>Long</td>
</tr>
<tr>
<td>23h</td>
<td>10 0011</td>
<td>Generic Short WRITE, 2 parameters</td>
<td>Short</td>
<td>2Eh</td>
<td>10 1110</td>
<td>Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format</td>
<td>Long</td>
</tr>
<tr>
<td>04h</td>
<td>00 0100</td>
<td>Generic READ, no parameters</td>
<td>Short</td>
<td>3Eh</td>
<td>11 1110</td>
<td>Packed Pixel Stream, 24-bit RGB, 8-8-8 Format</td>
<td>Long</td>
</tr>
<tr>
<td>14h</td>
<td>01 0100</td>
<td>Generic READ, 1 parameter</td>
<td>Short</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Example: CSI Packets

<table>
<thead>
<tr>
<th>Data Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00 – 0x07</td>
<td>Synchronization Short Packet Data Types</td>
</tr>
<tr>
<td>0x08 – 0x0F</td>
<td>Generic Short Packet Data Types</td>
</tr>
<tr>
<td>0x10 – 0x17</td>
<td>Generic Long Packet Data Types</td>
</tr>
<tr>
<td>0x18 – 0x1F</td>
<td>YUV Data</td>
</tr>
<tr>
<td>0x20 – 0x27</td>
<td>RGB Data</td>
</tr>
<tr>
<td>0x28 – 0x2F</td>
<td>RAW Data</td>
</tr>
<tr>
<td>0x30 – 0x37</td>
<td>User Defined Byte-based Data</td>
</tr>
<tr>
<td>0x38 – 0x3F</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Frame Start Code</td>
</tr>
<tr>
<td>0x01</td>
<td>Frame End Code</td>
</tr>
<tr>
<td>0x02</td>
<td>Line Start Code (Optional)</td>
</tr>
<tr>
<td>0x03</td>
<td>Line End Code (Optional)</td>
</tr>
<tr>
<td>0x04 – 0x07</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
CSI-2 Particulars

CCI – Camera Control Interface

• I2C subset used to configure camera interface (instead of BTA)
  – CCI is the protocol layer
  – Multiple-devices, single controller
• No BTA

Only HS transmissions

Simple Low-Level Protocol packet formats

• Long – for transmitting Application Specific Payload data
• Short – for transmitting Frame and Line synchronization data, and other image-related parameters.

Virtual Channel – independent data stream for one of up to four peripherals

1 packet per HS frame

• Frame Start/ Frame End
• Optional Line Start/ Line End
• LP State between frames
DSI Particulars

LPDT (on D0 only)
Low-power burst
Greater variety of packet types
- Short packets
- Long packets
- Processor commands (BTA)
- Great variety of image traffic
  - Burst (asynchronous)
  - Non-burst (synchronous, with and without sync events)
  - Display commands
Pixel Stream Types

**CSI**
- RGB888
- RGB666
- RGB565
- RGB555
- RGB444
- YUV422
- YUV420
- RAW 6/7/8/10/12/14

**DSI**
- RGB 12-12-12
- RGB 10-10-10
- RGB 8-8-8
- RGB 6-6-6
- RGB 5-6-5
- YCbCr 4-2-2
- YCbCr 4-2-0
Common pitfalls

Seldom related to signal integrity

Protocol timing
- Capturing data during settling time
- BTA collisions
- Adapting to bus speed changes

Lane misalignment
Non-burst image synchronization

Mitigation
- Intimate specification knowledge
- Corner case testing
- Protocol “omniscience”
Example: Start of Transmission timing error
## Look ahead at M-PHY

<table>
<thead>
<tr>
<th></th>
<th>D-PHY</th>
<th>M-PHY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Minimum configuration</strong></td>
<td>1-way or half-duplex CLK + DATA (4 pins)</td>
<td>dual-simplex DATA (4 pins)</td>
</tr>
<tr>
<td><strong>Min. pins for 6 Gbps</strong></td>
<td>10</td>
<td>4 (Gear 3)</td>
</tr>
<tr>
<td><strong>Data rate per lane</strong></td>
<td>HS: 80 Mbps to 1.5 Gbps LP: &lt;10 Mbps</td>
<td>HS: ~ 1.25/1.5; 2.5/3.0; 5/6 Gbps LP: 10k-600Mbps</td>
</tr>
<tr>
<td><strong>Electrical signaling</strong></td>
<td>HS LP</td>
<td>SLVS-200 LVCMOS1.2V</td>
</tr>
<tr>
<td><strong>HS Clocking method</strong></td>
<td>DDR Source-Sync Clk</td>
<td>Embedded</td>
</tr>
<tr>
<td><strong>HS Line coding</strong></td>
<td>None or 8b/9b</td>
<td>8b/10b</td>
</tr>
<tr>
<td><strong>Power – Energy/bit</strong></td>
<td>Low</td>
<td>Lower (YMMV)</td>
</tr>
<tr>
<td><strong>Repeater/optical</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>LP only PHY’s</strong></td>
<td>Disallowed</td>
<td>Allowed</td>
</tr>
</tbody>
</table>
Power Saving

Variable Gear Rates

- HS-3a/b (RT)
- HS-2a/b (RT)
- HS-1a/b (RT)
- Type-I Baseline Module (NT)
- PWM-0 (NT)
- PWM-1 (NT)
- PWM-2 (NT)
- PWM-3 (NT)
- PWM-4 (NT)
- PWM-5 (NT)
- PWM-6 (NT)
- PWM-7 (NT)

Power Saving Modes

<table>
<thead>
<tr>
<th>State</th>
<th>Recovery Latency</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIBERN8</td>
<td>0.1 – 1ms</td>
<td>10uW</td>
</tr>
<tr>
<td>Sleep</td>
<td>µs</td>
<td>100uW</td>
</tr>
<tr>
<td>LS Burst</td>
<td></td>
<td>1mW</td>
</tr>
<tr>
<td>Stall</td>
<td>ns</td>
<td>10mW</td>
</tr>
<tr>
<td>HS Burst</td>
<td></td>
<td>25mW</td>
</tr>
</tbody>
</table>

MIPI estimate for one M-TX and one M-RX including clock multiplication – v1.0
M-PHY Introduces a Transport Layer

Transport Layer
- Logical multiplexing of several communication channels (CPorts)
- E2E Flow Control

Network Layer
- Fully compatible with future Switched Network

Data Link Layer
- Link reliability
- Traffic Classes (TC0/TC1)

PHY Adapter Layer
- Abstraction of M-PHY
- Lane Discovery, downgrading
- Link Configuration (#lanes, gear etc.)
- Handling of multiple LANEs
- Native support for OMC